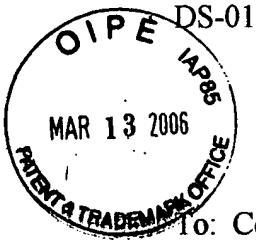
2838



DS-01-017

March 6, 2006

To: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
28 Davis Avenue
Poughkeepsie, NY 12603

Subject: Serial No. 10/042,073 01/08/02

Dirk Killat

CONVERTER WITH INDUCTOR AND DIGITAL CONTROLLED TIMING

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on March 9, 2006.

Stephen B. Ackerman, Reg. # 37761

Signature/Date 3/9/06

European Patent Application EP 0 582 813 A2 to Newton et al., "Critically Continuous Boost Converter," discusses continuous variable frequency boost converters.

European Patent Application EP 1 049 239 A1 to L'Hermite et al., "Power Factor Correction Controller Circuit," discusses a power factor correction controller circuit.

IBM Technical Disclosure Bulletin, Vol. 32, No. 9A, February 1990, pp. 35-37, Armonk, NY, USA, "Simulating Power Factor Correction Switching Converters Using Analog Models," discloses analog models that facilitate the simulation of a boost topology switching converter which can be used as a preprocessor to improve input power factor.

European Patent Application EP 0 792 006 A2 to Fiez, "Dc-to-Dc Switching Power Supply Utilizing a Delta-Sigma Converter in a Closed Loop Controller," discusses an improved DC-to-DC switching power supply which utilizes a delta-sigma converter in a closed loop controller.

European Patent Application EP 0 735 656 A2 to Canter et al., "Stabilized Power Converter Having Quantized Duty Cycle," discloses DC to DC power converters having a digital control loop that generates a quantized duty cycle.

"Fast Controller Design for Practical Power-Factor Correction Systems," by Wall et al., 0-7803-0891-3/93, 1999 IEEE, pp. 1027-1032, presents a fast controller for single-phase boost derived power-factor correction circuits.

Information in this Information Disclosure Statement was cited in a communication from a foreign Patent Office in a counterpart foreign application. The concise explanation of relevance for the non-English document is provided therein. A copy of that communication is attached:

Patent of Germany DE 37 01 089 C1 to Gemmel et al., "Verfahren zum Abgleichen der beiden Widerstande eines Spannungsteilers in einem Hybridschaltkreis."

Sincerely,

Stephen B. Ackerman,
Reg. No. 37761

Form PTO-1449

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
DS-01-017	10/042,073
Applicant: Dirk Killat	
Filing Date: 01/08/02	Group Art Unit:

U. S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO
EP05	8 2 8 1 3 A 2	6/22/93	European Patent App.	H02M	3/335		
EP1	0 4 9 2 3 9 A 1	4/30/99	European Patent App.	H02M	1/12		
EP07	9 2 0 0 6 A 2	2/20/97	European Patent App.	H02M	3/156		
EP07	3 5 6 5 6 A 2	3/28/96	European Patent App.	H02M	3/157		
DE 37	0 1 0 8 9 C 1	4/21/88	Germany	G01R	27/14		

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

- IBM Technical Disclosure Bulletin, Vol.32, No.9A, Feb.1990, pp. 35-37, Armonk, NY, USA, "Simulating Power Factor Correction Switching Converters Using Analog Models".
- "Fast Controller Design for Practical Power-Factor Correction Systems", by Wall et al., 0-7803-0891-3/93, 1999 IEEE, pp. 1027-1032.

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.